IN THE CLAIMS

Please amend the claims as follows:

1. (Currently amended) A power socket comprising:

a socket platform including a major planar surface; and on the socket platform:

a rectangular power terminal spaced apart from a rectangular ground terminal, wherein the power terminal includes a first cross-sectional area defined by a power terminal height by a power terminal width; and

an input/output (I/O) pin socket, wherein the I/O pin socket includes a second cross-sectional area that is smaller than the first cross-sectional area.

2. (Original) The power socket according to claim 1, on the socket platform further including:

a capacitor that has capacitor plates vertically oriented to the major planar surface.

3. (Original) The power socket according to claim 1, on the socket platform further including:

an inter-digital capacitor that has capacitor plates vertically oriented to the major planar surface.

4. (Original) The power socket according to claim 1, wherein the socket platform includes a first edge and a second edge, wherein the power terminal includes two power terminals, wherein the ground terminal includes two ground terminals, wherein the two power terminals are symmetrically disposed along the first edge, and wherein the two ground terminals are symmetrically disposed along the second edge.

5. (Original) The power socket according to claim 1, wherein the socket platform includes a first edge and a second edge, wherein the power terminal includes two power

terminals, wherein the ground terminal includes two ground terminals, wherein the two power terminals are symmetrically disposed along the first edge, wherein the two ground terminals are symmetrically disposed along the second edge; and

a capacitor that is vertically oriented to the major planar surface and that is disposed between one of the power terminals and one of the ground terminals.

6. (Original) The power socket according to claim 1, wherein the socket platform includes a first edge and a second edge, wherein the power terminal includes two power terminals, wherein the ground terminal includes two ground terminals, wherein the two power terminals are symmetrically disposed along the first edge, wherein the two ground terminals are symmetrically disposed along the second edge; and

a capacitor that is vertically oriented to the major planar surface and that is disposed either between the two power terminals or the two ground terminals.

7. (Original) The power socket according to claim 1, further:

wherein the socket platform includes a first edge and a second edge;

wherein the power terminal includes a first power terminal and a second power terminal;

wherein the ground terminal includes a first ground terminal and a second ground terminal;

wherein the capacitor includes a first capacitor and a second capacitor;

wherein the first and second power terminals are symmetrically disposed along the first edge;

wherein the first and second ground terminals are symmetrically disposed along the second edge;

wherein the first and second capacitors are vertically oriented to the major planar surface;

wherein the first capacitor is disposed between the first power terminal and the first ground terminal; and

wherein the second capacitor is disposed between the second power terminal and the second ground terminal.

8. (Original) The power socket according to claim 1, further:

wherein the socket platform includes a first edge and a second edge;

wherein the power terminal includes a first power terminal and a second power terminal;

wherein the ground terminal includes a first ground terminal and a second ground terminal;

wherein the capacitor includes a first capacitor and a second capacitor;

wherein the first and second power terminals are symmetrically disposed along the first edge;

wherein the first and second ground terminals are symmetrically disposed along the second edge;

wherein the first and second capacitors are vertically oriented to the major planar surface;

wherein the first capacitor is disposed between the first power terminal and the second power terminal; and

wherein the second capacitor is disposed between and the first ground terminal and the second ground terminal.

9. (Original) The power socket according to claim 1, wherein the I/O pin socket is part of a plurality of pin sockets.

10. (Currently amended) The power socket according to claim 1, on the socket platform further including:

a capacitor that has capacitor plates vertically oriented to the major planar surface, and wherein the capacitor includes an inter-digital capacitor of a first polarity type.

11. (Currently amended) The power socket according to claim 1, on the socket platform further including:

a capacitor that has capacitor plates vertically oriented to the major planar surface, and wherein the capacitor includes an inter-digital capacitor of a second polarity type.

12. (Currently amended) A power socket comprising:

a major planar upper surface and a major planar lower surface;

a rectangular power terminal spaced apart from a rectangular ground terminal, wherein the power terminal includes a first cross-sectional area defined by a power terminal height by a power terminal width;

a first plurality of input/output (I/O) pin sockets disposed at the major planar upper surface, wherein I/O pin socket of the plurality of I/O pin sockets includes a second cross-sectional area that is smaller than the first cross-sectional area;

a capacitor that has capacitor plates vertically oriented to the major planar surface; and

a second plurality of electrical bumps disposed at the major planar lower surface.

13. (Original) The power socket according to claim 12, wherein the second plurality of electrical bumps equals the first plurality of I/O pin sockets.

14. (Original) The power socket according to claim 12, wherein the capacitor includes an inter-digital capacitor.

15. (Original) The power socket according to claim 12, wherein the socket platform includes a first edge and a second edge, wherein the power terminal includes two power terminals, wherein the ground terminal includes two ground terminals, wherein the two power terminals are symmetrically disposed along the first edge, and wherein the two ground terminals are symmetrically disposed along the second edge.

16. (Original) The power socket according to claim 12, wherein the socket platform includes a first edge and a second edge, wherein the power terminal includes two power terminals, wherein the ground terminal includes two ground terminals, wherein the two power terminals are symmetrically disposed along the first edge, wherein the two ground terminals are symmetrically disposed along the second edge; and

wherein the capacitor includes a first and a second inter-digital capacitor that are vertically oriented to the major planar surface, and wherein the first inter-digital capacitor is disposed between one of the power terminals and one of the ground terminals.

17. (Currently amended) A power socket comprising:

a plurality of input/output (I/O) pin sockets embedded in a socket platform, wherein the socket platform includes a major planar surface;

a first power terminal embedded in the socket platform;

a ground terminal embedded in the socket platform; and

a capacitor embedded in the socket platform, wherein the capacitor includes a power plate and a ground plate, and wherein the power plate and the ground plate are configured orthogonal to the major planar surface.

18. (Original) The power socket according to claim 17, wherein the capacitor includes an inter-digital configuration.

19. (Original) The power socket according to claim 17, wherein the capacitor includes an inter-digital configuration including a plurality of power and ground plates, and wherein a given power plate and a given ground plate is spaced apart in a range from about 0.1 mils to about 0.5 mils.

20. (Original) The power socket according to claim 17, wherein the capacitor includes an inter-digital configuration including a plurality of power and ground plates, and the capacitor further including:

a series of alternating power and ground connectors disposed orthogonal to the power and ground plates.

21. (Original) The power socket according to claim 17, wherein the capacitor includes an inter-digital configuration including a plurality of power and ground plates, and the capacitor further including:

a series of four alternating power and ground connectors disposed orthogonal to the power and ground plates on a first side of the capacitor; and

a series of four alternating power and ground connectors disposed orthogonal to the power and ground plates on a second side of the capacitor, wherein the second side is opposite the first side.

22. (Original) The power socket according to claim 17, wherein the capacitor includes an inter-digital configuration including a plurality of power and ground plates, and the capacitor further including:

a series of four alternating power and ground connectors disposed orthogonal to the power and ground plates on a first side of the capacitor; and

a series of four alternating ground and power connectors disposed orthogonal to the power and ground plates on a second side of the capacitor, wherein the second side is opposite the first side, and wherein a given power connector on the first side is aligned opposite a given ground connector on the second side.

23. (Currently amended) The power socket according to claim 17, wherein the socket platform includes a first edge and a second edge that are parallel with the major planar surface, further including a second ~~wherein the~~ power terminal ~~includes two power terminals~~, wherein the ground terminal includes two ground terminals, wherein the first and second ~~two~~ power terminals are symmetrically disposed along the first edge, and wherein the two ground terminals are symmetrically disposed along the second edge.

24. (Currently amended) The power socket according to claim 17, wherein the socket platform includes a first edge and a second edge that are parallel with the major planar surface, further including a second ~~wherein the~~ power terminal ~~includes two power terminals~~, wherein the ground terminal includes two ground terminals, wherein first and second ~~two~~ power terminals are symmetrically disposed along the first edge, wherein the two ground terminals are symmetrically disposed along the second edge; and

wherein the capacitor that is vertically oriented to the major planar surface is disposed between one of the power terminals and one of the ground terminals.

25. (Original) The power socket according to claim 17, wherein the socket platform includes a first edge and a second edge that are parallel with the major planar surface, wherein the power terminal includes two power terminals, wherein the ground terminal includes two ground terminals, wherein the two power terminals are symmetrically disposed along the first edge, wherein the two ground terminals are symmetrically disposed along the second edge; and

wherein the capacitor that is vertically oriented to the major planar surface and is disposed either between the two power terminals or the two ground terminals.

26. (Withdrawn) A method of operating a device, comprising:

passing a current through a power socket, wherein an alternating first current passes in a first direction through a first capacitor plate that is configured in a plane collinear with the first direction;

wherein a direct second current passes in the first direction through a power terminal;

wherein the alternating first current discharges into a second capacitor plate in a second direction that is substantially opposite to the first direction, wherein the second capacitor plate is spaced apart and immediately adjacent the first capacitor plate; and

wherein the direct second current passes to ground through a ground terminal in the second direction.

27. (Withdrawn) The method according to claim 26, wherein the first capacitor plate and the second capacitor plate are interdigitally configured.

28. (Withdrawn) The method according to claim 26, further including:

while increasing frequency in a power signal, initiating a lowered inductance path through the first capacitor plate and the second capacitor plate.